PTO/SB/64 (09-04)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT ABANDONED UNINTENTIONALLY UNDER 37 CFR 1.137(b)

Docket Number (Optional): 111027-141513

First named inventor: Brian D. Possley

Application No.: 09/262,458 Art Unit: 2814

Filed: 03/04/1999 Examiner: Ngo, Ngan V.

Title: GATE ARRAY ARCHITECTURE

Attention: Office of Petitions
Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
FAX (703) 872-9306

NOTE: If information or assistance is needed in completing this form, please contact Petitions Information at (703) 305-9282.

The above-identified application became abandoned for failure to file a timely and proper reply to a notice or action by the United States Patent and Trademark Office. The date of abandonment is the day after the expiration date of the period set for reply in the office notice or action plus an extensions of time actually obtained.

APPLICANT HEREBY PETITIONS FOR REVIVAL OF THIS APPLICATION

NOTE: A grantable petition requires the following items:
(1) Petition fee;
(2) Reply and/or issue fee;
(3) Terminal disclaimer with disclaimer fee - required for all utility and plant applications filed before June 8, 1995; and for all design applications; and
(4) Statement that the entire delay was unintentional.

1. Petition fee

☐ Small entity-fee $ _____ (37 CFR 1.17(m)). Applicant claims small entity status. See 37 CFR 1.27.

☑ Other than small entity – fee $ 1500.00 (37 CFR 1.17(m))

2. Reply and/or fee

A. The reply and/or fee to the above-noted Office action in the form of RCE, Amendment, and Petition for Extension of Time (identify type of reply):

☐ has been filed previously on _____.
☑ is enclosed herewith.

06/06/2005 MAHMED1 00000065 09262458
01 FC:1453 1500.00 OP

B. The issue fee and publication fee (if applicable) of $ _____.

☐ has been paid previously on _____.
☐ is enclosed herewith.

3. Terminal disclaimer with disclaimer fee

☐ Since this utility/plant application was filed on or after June 8, 1995, no terminal disclaimer is required.

☐ A terminal disclaimer (and disclaimer fee (37 CFR 1.20(d)) of $ _____ for a small entity or $ _____ for other than a small entity) disclaiming the required period of time is enclosed herewith (see PTO/SB/63).

4. STATEMENT: The entire delay in filing the required reply from the due date for the required reply until the filing of a grantable petition under 37 CFR 1.137(b) was unintentional. [NOTE: The United States Patent and Trademark Office may require additional information if there is a question as to whether either the abandonment or the delay in filing a petition under 37 CFR 1.137(b) was unintentional (MPEP 711.03(c), subsections (III)(C) and (D)).]

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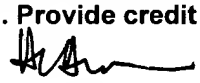


Signature — 06/01/2005 — Date

Aloysius T.C. AuYeung — Typed or printed name

35432 — Registration Number, if applicable

Pacwest Center, Suite 1900 — Address

503-222-9981 — Telephone Number

1211 SW Fifth Ave., Portland, OR 97204 — Address

Enclosures:
- ☑ Fee Payment
- ☑ Reply
- ☐ Terminal Disclaimer Form
- ☐ Additional sheets containing statements establishing unintentional delay
- ☑ Other: Petition for Extension of Time

CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(a)]

I hereby certify that this correspondence is being:

☑ Deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Petition, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.

☐ Transmitted by facsimile on the date shown below to the United States Patent and Trademark Office as (703) 872-9306.

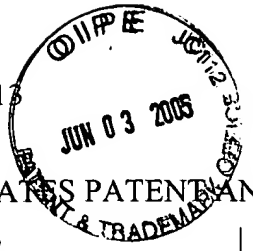
06/01/2005 — Date

Signature

Heather L. Adamson — Typed or printed name of person signing certificate

Attorney Docket No. 111027-141513
IPN P06643 (Intel Corporation)

Patent



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	09/262,458
Applicant	Brian D. Possley
Filed	March 4, 1999
TC/ A/U.	2814
Examiner	Ngo, Ngan V.
Attorney Docket No.	111027-141513
Confirmation No.	9423

CERTIFICATE OF TRANSMISSION / MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Typed or Printed: Heather h. Adamson

Signature: _____ Date: 06/01/2005

Attention: Office of Petitions
Mail Stop Petition
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

PETITION FOR REVIVAL AND

AMENDMENT ACCOMPANYING REQUEST FOR CONTINUED EXAMINATION

Dear Examiner Ngo:

In response to the Final Office Action mailed April 7, 2004, Applicant respectfully requests reconsideration of the captioned application in view of the following:

Amendments to the Claims – begin on page 2 of this paper; and

Remarks/Arguments – begin on page 6 of this paper.

Applicant hereby petitions for revival of the above referenced application, and has enclosed with this submission a Petition for Revival of an Application for Patent Abandoned Unintentionally Under 37 CFR 1.137(b). The entire delay in filing the required reply from the due date for the required reply until the filing of a grantable petition under 37 CFR 1.137(b) was unintentional.

Additionally, it is requested that the Attorney Docket No. be changed to 111027-141513.

AMENDMENTS TO THE CLAIMS

Please amend the claims as set forth below:

What is claimed is:

1.-6. (Canceled)

7. (Currently amended) The integrated circuit of claim 456, wherein the adjacently disposed stripes of adjacently disposed arrangements of first and second size transistors are ~~said gate array architecture is~~ repeated in a pattern in said integrated circuit.

8. (Currently amended) The integrated circuit of claim 456, wherein said integrated circuit is ~~incorporated in~~ a communications integrated circuit~~device~~.

9. (Currently amended) The integrated circuit of claim 456, wherein said integrated circuit further comprises a plurality of terminals designed to enable the integrated circuit to be packaged for ~~is~~ attachment~~ed~~ to a motherboard.

10. (Currently amended) The integrated circuit of claim 9, wherein said motherboard is a motherboard of a computing device ~~said integrated circuit is incorporated in a personal computer~~.

11. (Currently amended) The integrated circuit of claim 10, wherein said ~~personal~~ computing~~er~~ device comprises one of a laptop computer and a desktop computer.

12.-44. (Canceled)

45. (New) An integrated circuit comprising:

a plurality of arrangements of first size transistors adjacently disposed along a first stripe of substrate area, each arrangement of first size transistors having one or more pairs of a first size p-type transistor and a first size n-type transistor;

first one or more interconnects interconnecting exclusively first size transistors of one or more adjacent ones of the plurality of arrangements of first size transistors to form a clock buffer of a logic component, consisting exclusively of first size transistors;

a plurality of arrangements of second size transistors adjacently disposed along a second stripe of substrate area adjacently disposed parallel to the first stripe of substrate area, each arrangement of second size transistors having one or more pairs of a second size p-type transistor and a second size n-type transistors; and

second one or more interconnects interconnecting exclusively second size transistors of one or more adjacent ones of the plurality of arrangements of second size transistors to form a logic element of the logic component, consisting exclusively of second size transistors.

46. (New) The integrated circuit of claim 45, wherein the second size transistors are full size transistors.

47. (New) The integrated circuit of claim 46, wherein the first size transistors are smaller than the second size transistors.

48. (New) The integrated circuit of claim 45, wherein the first size transistors are smaller than the second size transistors.

49. (New) The integrated circuit of claim 45, wherein a ratio between the second size transistors and the first size transistors is on an order of one-third.

50. (New) The integrated circuit of claim 45, wherein a ratio between capacitance of the second size transistors and the first size transistors is on an order of one-third.

51. (New) The integrated circuit of claim 45, wherein the logic element has a higher power consumption characteristic than the clock buffer.

52. (New) The integrated circuit of claim 45, wherein the logic component comprises a flip-flop.

53. (New) The integrated circuit of claim 45, wherein the logic element is designed to perform an operation selected from the group consisting of a multiplexing operation, a NAND operation, an AND operation, a NOR operation, and an OR operation.

54. (New) An article comprising:

a storage medium; and

a plurality of instructions stored in the storage medium, the instructions designed to enable an apparatus to design a layout of an integrated circuit for fabrication, the integrated circuit having

a plurality of arrangements of first size transistors adjacently disposed along a first stripe of substrate area, each arrangement of first size transistors having one or more pairs of a first size p-type transistor and a first size n-type transistor,

first one or more interconnects interconnecting exclusively first size transistors of one or more adjacent ones of the plurality of arrangements of first size transistors to form a clock buffer of a logic component, consisting exclusively of first size transistors,

a plurality of arrangements of second size transistors adjacently disposed along a second stripe of substrate area adjacently disposed parallel to the first stripe of substrate area, each arrangement of second size transistors having one or more pairs of a second size p-type transistor and a second size n-type transistors, and

second one or more interconnects interconnecting exclusively second size transistors of one or more adjacent ones of the plurality of arrangements of second size transistors to form a logic element of the logic component, consisting exclusively of second size transistors.

55. (New) The article of claim 54, wherein the second size transistors are full-size transistors.

56. (New) The article of claim 55, wherein the first size transistors are smaller than the second size transistors.

57. (New) The article of claim 56, wherein the clock buffer consumes less power than the logic element.

58. (New) The article of claim 54, wherein the first size transistors are smaller than the second size transistors.

59. (New) The article of claim 58, wherein the clock buffer consumes less power than the logic element.

REMARKS/ARGUMENTS

I. Claim Amendments

Claims 1-6, 21-26 and 44 have been canceled, without prejudice (claims 12-20 and 27-43 having previously been canceled). Claims 7-11 have been amended. Claims 45-59 are newly submitted. The amended and newly submitted claims are fully supported by the original disclosure and no new matter has been introduced.

II. Claim Rejections under 35 U.S.C. §103(a)

In the subject Office Action, claims 1-11, 21-26, and 44 were rejected under 35 U.S.C. 103(a) as being unpatentable over Sato in view of Tran et al ("Tran") and Faue et al ("Faue"). Applicant has canceled claims 1-6, 21-26 and 44, without prejudice, rendering the rejections to these claims moot. Claims 7-11 have been amended to depend from newly submitted claim 45, resulting in claims 7-11 all depending, directly or via intervening claims, from newly submitted claim 45. For reasons to be discussed in more detail below, claim 45 is patentable over the cited references. Accordingly, for at least the same reasons, claims 7-11 are patentable over the cited references.

III. New Claims

Newly submitted independent claim 45 is patentable over the cited references because none of the cited references individually or in combination teaches or suggests the required

> a plurality of arrangements of first size transistors adjacently disposed along a first stripe of substrate area, each arrangement of first size transistors having one or more pairs of a first size p-type transistor and a first size n-type transistor;
>
> first one or more interconnects interconnecting exclusively first size transistors of one or more adjacent ones of the plurality of arrangements of first size transistors to form a clock buffer of a logic component, consisting exclusively of first size transistors.

In particular, Sato merely teaches of disposition of a column of basic cells of larger size transistors, in between two columns of basic cells of standard size transistor, wherein interconnects are provided to interconnect standard size and larger size transistors of basic cells

of adjacently disposed columns, to form a clock buffer with transistors of two sizes, standard size as well as larger size transistors.

Accordingly, claim 45 is patentable over the cited references.

Claim 54 contains in substance the same recitation of claim 45. Accordingly, for at least the same reasons, claim 54 is patentable over the cited references.

Claims 46-53 and 55-59 depend from claims 45 and 54, incorporating their recitations respectively. Accordingly, for at least the same reasons, claims 46-53 and 55-59 are patentable over the cited references.

IV. Conclusion

In view of the foregoing, Applicant submits all remaining pending claims, i.e., claims 7-11 and 45-59, are in condition of allowance. Issuance of the Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge shortages or credit overpayments of Fees to Deposit Account No. 500393.

Respectfully submitted,
SCHWABE, WILLIAMSON & WYATT, P.C.

Dated: June 1, 2005

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